

WHAT IS CLAIMED IS :

Sub A1  
1. A method for reducing an importance level of a line in a memory of a cache, the method comprising providing an instruction to the cache indicating that the line is a candidate for replacement.

Sub B1  
2. The method as recited in claim 1 further comprising reducing an importance level of the line based on the instruction.

Sub A2  
3. The method as recited in claim 2 wherein the reducing of the importance level of the line results in the line being replaced prior to another line scheduled for replacement by a replacement policy of the cache.

Sub B2  
4. The method as recited in claim 3 wherein the replacement policy is a least recently used policy and wherein the other line is less recently used than the line.

Sub B3  
5. The method as recited in claim 1 further comprising altering an allocation methodology of the cache based on the instruction.

Sub A3  
6. The method as recited in claim 1 wherein the instruction is in part of an application kernel.

Sub B4  
7. The method as recited in claim 1 wherein the instruction is generated by a compiler.

8. The method as recited in claim 1 wherein the instruction is an extension of a memory access instruction.

Sub  
A4

1  
2

9. ~~A instruction for increasing hit rate of a cache, the instruction comprising an indication that a line in a memory of the cache is a candidate for replacement.~~

Sub  
B1

1  
2

10. ~~The instruction as recited in claim 9 wherein the indication causes a reduction of an importance level of the line.~~

Sub  
A5

1  
2  
3

11. ~~The instruction as recited in claim 10 wherein the reducing of the importance level of the line results in the line being replaced prior to another line scheduled for replacement by a replacement policy of the cache.~~

Sub  
B1

1  
2

12. ~~The instruction as recited in claim 11 wherein the replacement policy is a least recently used policy and wherein the other line is less recently used than the line.~~

1  
2

13. The instruction as recited in claim 9 further comprising altering an allocation methodology of the cache based on the instruction.

1  
2

14. The instruction as recited in claim 9 wherein the instruction is in part of an application kernel.

1  
2

15. The instruction as recited in claim 9 wherein the instruction is generated by a compiler.

1  
2

16. The instruction as recited in claim 9 wherein the instruction is an extension of a memory access instruction.

Sub  
A5

1  
2  
3

17. ~~An article comprising a storage medium, the storage medium having a set of instructions, the set of instructions being capable of being executed by at least one processor to implement a method for reducing an importance level of a line in a memory of~~

4 ~~a cache, the set of instructions when executed comprising providing an indication to the~~  
5 ~~cache that the line is a candidate for replacement.~~

Sub A5  
Sub B1  
1 18. The article as recited in claim 17 wherein the set of instructions further comprises  
2 reducing an importance level of the line based on the indication.

Sub A6  
1 19. The article as recited in claim 18 wherein the reducing of the importance level of  
2 the line results in the line being replaced prior to another line scheduled for replacement by  
3 a replacement policy of the cache.

Sub B1  
1 20. The article as recited in claim 19 wherein the replacement policy is a least recently  
2 used policy and wherein the other line is less recently used than the line.

1 21. The article as recited in claim 17 further comprising altering an allocation  
2 methodology of the cache based on the indication.

1 22. The article as recited in claim 17 wherein the indication is part of an application  
2 kernel.

1 23. The article as recited in claim 17 wherein the indication is generated by a compiler.

1 24. The article as recited in claim 17 wherein the indication is an extension of a  
2 memory access instruction.

Sub A7  
1 25. A cache comprising:  
2 a cache memory including a cache line; and  
3 a cache control logic for reducing an importance level of the cache line based on an  
4 instruction.

Sub  
B1

1 26. The cache as recited in claim 25 wherein the instruction provides an indication that  
2 the cache line is a candidate for replacement.

1 27. The cache as recited in claim 26 wherein the cache control logic reduces an  
2 importance level of the cache line based on the indication.

1 28. The cache as recited in claim 27 wherein the reducing of the importance level of the  
2 cache line results in the cache line being replaced prior to another cache line scheduled for  
3 replacement by a replacement policy of the cache.

1 29. The cache as recited in claim 25 further comprising altering an allocation  
2 methodology of the cache based on the instruction.

1 30. A method for reducing an importance level of a line in a memory of a cache, the  
2 method comprising:

3 providing an instruction to the cache indicating that the line is a candidate for  
4 replacement; and

5 reducing an importance level of the line based on the instruction.